**Experiment – 8**

**Verilog code for designing D Flip Flop.**

**design.sv**module D\_flipflop(CLK, D, Q);  
 input CLK, D;  
 output reg Q;  
  
 always @(posedge CLK) begin  
 Q <= D;  
 end   
endmodule

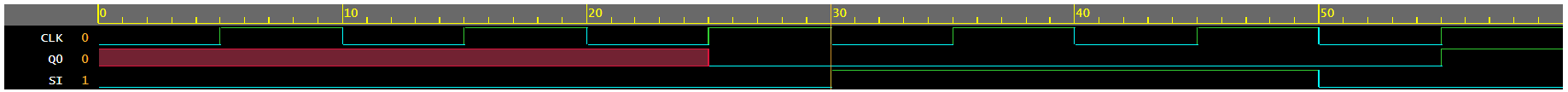
**Verilog code for designing a SISO Shift Register using D Flip Flop.**

**design.sv**module SISO(CLK, SI, Q0);  
 input CLK, SI;  
 output Q0;  
 wire Q2, Q1;  
  
 D\_flipflop FF0 (CLK, SI, Q2);  
 D\_flipflop FF1 (CLK, Q2, Q1);  
 D\_flipflop FF2 (CLK, Q1, Q0);  
endmodule

**testbench.sv**module SISO\_test;  
 reg CLK, SI;  
 wire Q0;  
  
 SISO SISO\_dut (CLK, SI, Q0);  
  
 initial begin  
 CLK = 0;  
 forever #5 CLK = ~CLK;  
 end  
   
 initial begin  
 SI = 0; #10;  
 SI = 0; #10;  
 SI = 0; #10;  
 SI = 1; #10;  
 SI = 1; #10;  
 SI = 0; #10;  
 $finish;  
 end

initial begin  
 $dumpfile("test.vcd");  
 $dumpvars(1, SISO\_test);  
 end  
endmodule

**Output Waveform**

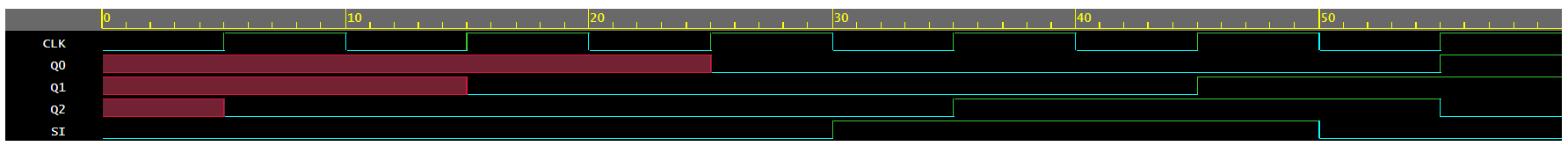


**Verilog code for designing a SIPO Shift Register using D Flip Flop.**

**design.sv**module SIPO(CLK, SI, Q2, Q1, Q0);  
 input CLK, SI;  
 output Q2, Q1, Q0;  
  
 D\_flipflop FF0 (CLK, SI, Q2);  
 D\_flipflop FF1 (CLK, Q2, Q1);  
 D\_flipflop FF2 (CLK, Q1, Q0);  
endmodule

**testbench.sv**module SIPO\_test;  
 reg CLK, SI;  
 wire Q2, Q1, Q0;  
  
 SIPO SIPO\_dut (CLK, SI, Q2, Q1, Q0);  
  
 initial begin  
 CLK = 0;  
 forever #5 CLK = ~CLK;  
 end  
   
 initial begin  
 SI = 0; #10;  
 SI = 0; #10;  
 SI = 0; #10;  
 SI = 1; #10;  
 SI = 1; #10;  
 SI = 0; #10;  
 $finish;  
 end  
  
 initial begin  
 $dumpfile("test.vcd");  
 $dumpvars(1, SIPO\_test);  
 end  
endmodule

**Output Waveform**

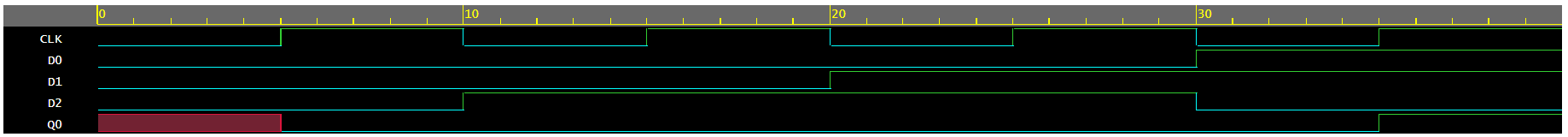


**Verilog code for designing a PISO Shift Register using D Flip Flop.**

**design.sv**module PISO(CLK, D2, D1, D0, Q0);  
 input CLK, D2, D1, D0;  
 output Q0;  
 wire Q2, Q1;  
  
 D\_flipflop FF0 (CLK, D2, Q2);  
 D\_flipflop FF1 (CLK, D1, Q1);  
 D\_flipflop FF2 (CLK, D0, Q0);  
endmodule

**testbench.sv**module PISO\_test;  
 reg CLK, D2, D1, D0;  
 wire Q0;  
  
 PISO PISO\_dut (CLK, D2, D1, D0, Q0);  
  
 initial begin  
 CLK = 0;  
 forever #5 CLK = ~CLK;  
 end  
   
 initial begin  
 {D2, D1, D0} = 3'b000; #10;  
 {D2, D1, D0} = 3'b100; #10;  
 {D2, D1, D0} = 3'b110; #10;  
 {D2, D1, D0} = 3'b011; #10;  
 $finish;  
 end  
  
 initial begin  
 $dumpfile("test.vcd");  
 $dumpvars(1, PISO\_test);  
 end  
endmodule

**Output Waveform**



**Verilog code for designing a PIPO Shift Register using D Flip Flop.**

**design.sv**module PIPO(CLK, D2, D1, D0, Q2, Q1, Q0);  
 input CLK, D2, D1, D0;  
 output Q2, Q1, Q0;  
  
 D\_flipflop FF0 (CLK, D2, Q2);  
 D\_flipflop FF1 (CLK, D1, Q1);  
 D\_flipflop FF2 (CLK, D0, Q0);  
endmodule

**testbench.sv**module PIPO\_test;  
 reg CLK, D2, D1, D0;  
 wire Q2, Q1, Q0;  
  
 PIPO PIPO\_dut (CLK, D2, D1, D0, Q2, Q1, Q0);  
  
 initial begin  
 CLK = 0;  
 forever #5 CLK = ~CLK;  
 end  
   
 initial begin  
 {D2, D1, D0} = 3'b000; #10;  
 {D2, D1, D0} = 3'b100; #10;  
 {D2, D1, D0} = 3'b110; #10;  
 {D2, D1, D0} = 3'b011; #10;  
 $finish;  
 end  
  
 initial begin  
 $dumpfile("test.vcd");  
 $dumpvars(1, PIPO\_test);  
 end  
endmodule

**Output Waveform**

